33.2 A Multi-Band Multi-Mode CMOS Direct-Conversion DVB-H Tuner

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The mobile TV applications including DVB-H, DMB, ISDB-T solutions that have been launched recently, draw many research efforts to make low-cost high-performance tuner chip set, which in-turn, push designers to use low-cost CMOS technologies and direct-conversion architecture [1, 2, 3]. The DVB-H tuner, presented in this paper, supports UHF band (470 to 862MHz) and USA-L band (1670 to 1675MHz) and uses direct-conversion architecture for reducing the number of external components. As shown in Fig. 33.2.1, most blocks such as LNAs, mixers, VGAs, filters, PLL, and all external passive components are integrated except the matching circuits for LNAs and the inductor for VCO2. In addition, the integrated active balun, right after the front-end LNA, makes the application simple. The IC is implemented in a 0.18μm 40GHz-f_T CMOS technology.

The front-end part in the receiver decides, generally, the NF and IP3 of the receiver. The baseband part performs filtering, dc-offset cancellation (DCOC), and changing the gain, without degrading the system performance. If the CMOS device is used in the down-conversion mixer, the 1/f noise of the down-conversion mixer makes a considerable impact on NF of the total system. Thus, the 1/f noise is the criterion of gain budget. In case of the relatively high IP3 requirement for the DVB-H system, the gain of the front-end cannot be high. This low-gain front-end block requires the high performance of the following blocks in order to satisfy the noise performance. If there is a low 1/f noise device in a CMOS technology, it is easier to achieve the high IP3 and low NF, simultaneously. The LNA adopts the cascode type with parallel resistive feedback to cover the wideband operation. To minimize the effects of 1/f noise, switching stage of mixer, 1st VGA and 2nd VGA are implemented with new vertical BJT, which is fabricated by adding an additional p-base implant in deep n-well in the CMOS process. Figure 33.2.2 shows the NF performance of the full path. There is not any noise slope around zero frequency and the measured Y-factor from the band power measurement at 666MHz is 10.7, which means NF=4.3dB with compensated 0.2dB loss. By adding one base mask for changing the doping density, the vertical BJT is easily created. The vertical BJT shows superior 1/f noise performance, β=35, and f_T=5GHz. The rest of the blocks in the path are implemented using CMOS devices for a compact layout.

The gain of the receiver can be varied from 2dB to 95.2dB at 0.5dB steps. The full path NF of 4.5/5dB in UHF/USA-L band is achieved at a 64dB gain setting, respectively. For the same gain setting, a 16MHz-offset IIP3 of –5/–6dBm in UHF/USA-L is measured, respectively. An IIP2 performance up to 40dBm is achieved without IP2 calibration. The sensitivity performance of the DVB-H tuner is closely related with the performance of the demodulator, which is implemented by in an FPGA. As shown in Fig. 33.2.3, the measured sensitivity is –89dBm at 16QAM and CR (code rate)=1/2.

The LPF block is distributed throughout the receiver chain to meet the channel selectivity and blocker requirements. The first two LPFs are implemented with 1st-order RC filters. A 6th-order active-RC filter is followed by a 2nd-order equalizer. To compensate process- and temperature-dependant pole variations, the auto-calibration algorithm is used for adjusting the capacitors. To cover 5/6/7/8MHz channel space, the nominal capacitance of the filter is switched for selecting the proper bandwidth according to each application. The measured filter mask, which gives more than 30dB rejection at 1.25MHz- offset, is shown in Fig. 33.2. 4. DCOC loops accompany each of the two VGAs. The settling time of DCOC loops should be short as it can, because the DVB-H tuner turns on for once per ten slots. Additionally, the cancellation should be reserved for a long time. The corner frequency of DCOC is intentionally increased to more than 20kHz when the tuner is turned on, and decreased back to 1kHz after 200μs. In order to reduce the chip area, it is important to obtain small transconductance, which reduces the area required by the low-corner frequency capacitance. Using the active transconductance, a corner frequency of less than 1kHz is achieved with reasonable capacitance. The worst settling time is 140μs, as shown in Fig. 33.2.5.

The synthesizer consists of two functional loops of a PLL and a frequency-lock loop. An adaptive frequency calibration (AFC) block is needed for tuning the VCO near the target frequency prior to the start of phase lock. A 3b 4th-order ΔΣ fractional-N synthesizer with integrated VCO is incorporated. The VCOs for UHF/USA-L band have a tuning range of 890 to 1815/3100 to 3650MHz with a loop bandwidth of around 20kHz, respectively. The measurements show that the in-band phase noise is to be –80.5/-78.5dBc/Hz and the out-band phase noise is –99.2/-98.1dBc/Hz at a 100kHz offset, in the respective 1420/3345MHz frequency. Within the synthesizer, is an adaptive frequency calibrator that helps to guarantee a lock time of less than 300μs. The synthesizer can handle the reference signals of 13/19.2/26/38.4MHz.

To reduce the chip area, the lead-frames and external inductor are used as tank inductors for UHF band VCO and the bond-wires are used as inductors for the USA-L band VCO. The 5b capacitor banks of VCO for the UHF band mode are composed of MIM capacitors and MOS switch, and the 5b capacitor banks of VCO for the USA-L band are composed of accumulation-MOS varactor and MOS switch. To reduce the noise interaction between blocks, a 2.4V regulator is adopted for VCOs and a 1.8V regulator for the PLL. The regulator for VCO is designed to have the low output noise not to make an effect on the phase noise. The vertical BJT is employed in the proportional-to-absolute-temperature (PTAT) circuit of this regulator.

The rejection of the LPF at the 1.25MHz offset is more than 30dB. The rest of the filter rejection for satisfying the PAL-rejection requirement is performed in the demodulator. The PAL rejection at (N-1)/(N+1) with 16QAM and CR=2/3 is measured as 41.5/38.9dB, respectively. The current consumption of the tuner with 2.8V is 66mA for UHF band, and 74mA for USA-L band. In Figure 33.2.6, the tuner performance is summarized. The micrograph of the tuner is shown in Fig. 33.2.7.

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References:
[1] S. Azuma, et al., "A Digital Terrestrial Television(ISDB-T) Tuner for Mobile Application," *ISSCC Dig. Tech. Papers*, pp. 278-279, Feb., 2004.
[2] Chun-Huat, H, et al., "A CMOS TV Tuner/Demodulator IC with Digital Image Rejection," *ISSCC Dig. Tech. Papers*, pp. 432-433, Feb., 2005.
[3] P. Antoine, et al., "A Direct-Conversion Receiver for DVB-H," *ISSCC Dig. Tech. Papers*, pp. 426-427, Feb., 2005.

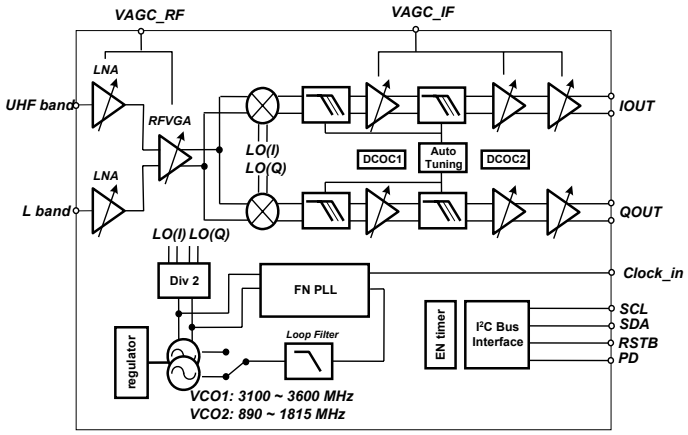
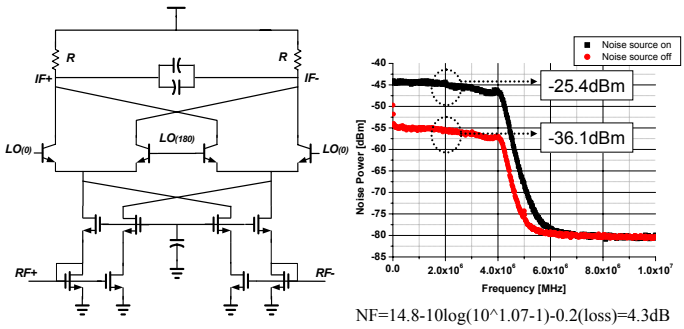


Figure 33.2.1: DVB-H block diagram.



NF=14.8-10log(10^1.07-1)-0.2(loss)=4.3dB

Figure 33.2.2: Mixer schematic including vertical BJT and full-path NF.

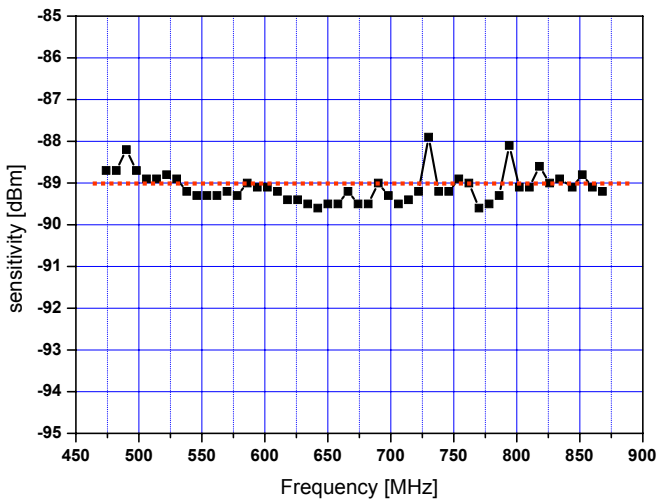


Figure 33.2.3: Measured sensitivity (16QAM, CR=1/2).

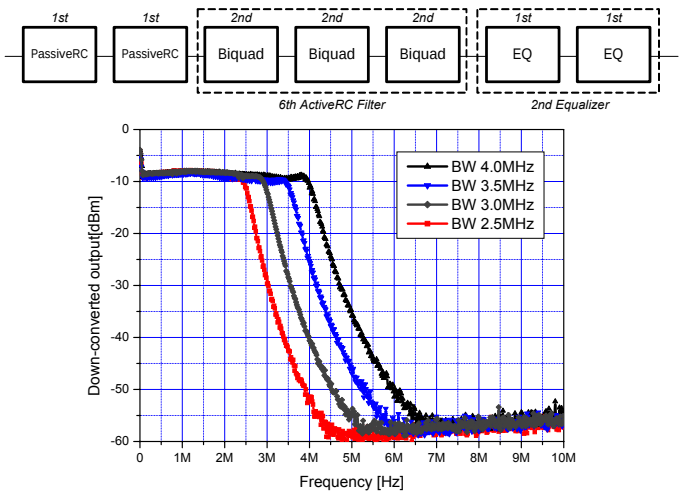


Figure 33.2.4: LPF block diagram and filter mask.

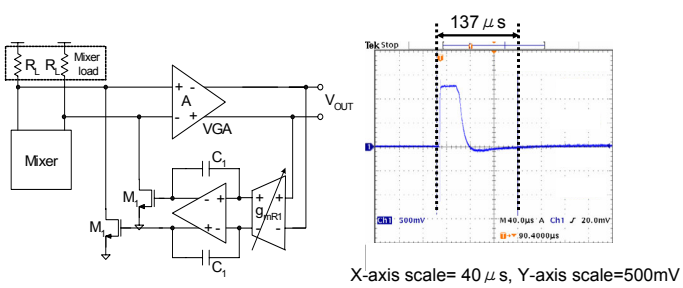


Figure 33.2.5: DCOC schematic and measured settling time: settling time=137μs.

Operating range	470 ~ 850	1670 ~ 1675	MHz
Bandwidth	3/3.5/4	2.5	MHz
NF @ gain = 64dB	4.5	5	dB
IIP3@ gain = 64dB	-5	-6	dBm
IIP2@ gain = 64dB	> 40		dBm
Phase noise@RFx2	-80.5 @ <10kHz -99.2 @ 100kHz -127.2 @ 1.25MHz	-78.5 @ <10kHz -98.1 @ 100kHz -122.3 @ 1.25MHz	dBc/Hz
Gain DR	95.2	94.2	dB
PAL rejection(using Demodulator)	41.5 @ N-1, 38.9 @ N+1		dB
I/Q gain mismatch	< 0.5		dB
I/Q phase mismatch	< 2		dgeree
Settling time	DCOC < 140 Synthersizer < 300		μs
Sensitivity(16QAM,CR=1/2)	-89	-88.5	dBm
Power consumption (2.8V)	66	74	mA

Figure 33.2.6. Measured performance summary.

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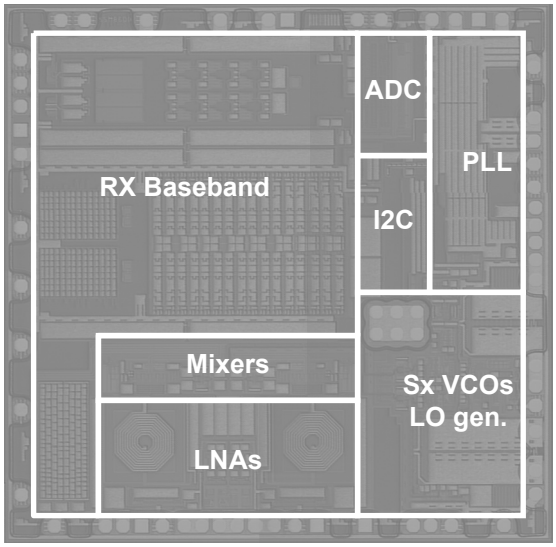

Figure 33.2.7: Die micrograph of the IC: 2800μm x 2800μm.

